Notice of Allowability	Application No.	Applicant(s)	
	09/363,605	LABERGE, PAUL A.	
	Examiner	Art Unit	
	Xuong M. Chung-Trans	2833	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the appeal brief filed on November 19, 2003*.
2. ☒ The allowed claim(s) is/are *1-9, 11-16, 18-23 and 26-28 and now as 1-24*.
3. ☒ The drawings filed on *29 July 1999* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No. 2.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the margin according to 37 CFR 1.121(d).

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachm nt(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No. _____
4☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5☐ Notice of Informal Patent Application (PTO-152)
6☒ Interview Summary (PTO-413), Paper No. *1/15/04*.
7☒ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .

1. An **examiner's amendment** to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Fred Pruner, Jr. on January 16, 2004.

2. The application has been amended as follows:

1. (Currently Amended) A computer system comprising:
a local bus;
a memory bus capable of indicating data; ~~and~~
a first buffer adapted to capture the data directly from the memory bus, the buffer being located closer to the local bus than to the memory bus; and
a memory interface located closer to the memory bus than to the local bus, the memory interface including a second buffer to store other data to be furnished to the memory bus.

2. (Currently Amended) The computer system of claim 1, wherein
the memory bus is capable of indicating a data strobe signal, and
the first buffer is adapted to latch the data from the memory bus in response to the data strobe signal.

3. (Currently Amended) The computer system of claim 1, further comprising:
conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the first buffer to a second region located closer to the first buffer than to the memory bus, the conductive traces introducing an approximate first asynchronous propagation delay in the communication.

4. (Currently Amended) The computer system of claim 3, further comprising:
circuitry adapted to transfer the data from the first buffer to the local bus without introducing a second propagation asynchronous propagation delay that is greater than the first asynchronous propagation delay.

5. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface.

6. (Currently Amended) The computer system of claim 1, further comprising:
circuitry adapted to transfer the data from the first buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clack signal.

7. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface that is coupled to the local bus, the computer system further comprising:
a third bus;
a fourth bus;
a third bus interface coupled to communicate with the third bus;
a fourth bus interface coupled to communicate with the fourth bus; and
a multiplexing circuit adapted to selectively cause the first buffer to store other data from the third and fourth bus interfaces.

8. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface that is located closer to the local bus than to the memory bus.

9. (Original) The computer system of claim 8, wherein the local bus interface further comprises:
a local bus controller adapted to use the first buffer to furnish sisals to the local bus that indicate the data.

10. (Cancelled)

11. (Currently Amended) A bridge for use with a local bus and a memory bus capable of indicating data, comprising:
conductive traces adapted to communicate indications of the data from a first region closer to the memory bus than the local bus to a second region located closer to the local bus
than to the memory bus; ~~and~~
a local bus interface being located closer to the local bus than to the memory bus, the local bus interface including a first buffer adapted to capture the indications of

the data from the conductive traces near the second region to directly capture the data from the memory bus; and

a memory interface located spatially closer to the memory bus than to the local bus, the memory interface including a second buffer to store other data to be furnished to the memory bus.

12. (Currently Amended) The bridge of claim 11, wherein
the memory bus is capable of indicating a data strobe signal, and
the first buffer is adapted to latch the data in response to the data strobe signal.

13. (Currently Amended) The bridge of claim 11, wherein the conductive traces introduce a first asynchronous propagation delay to the indications of the data, the bridge further comprising:

circuitry adapted to transfer the data from the first buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

14. (Currently Amended) The bridge of claim 13, further comprising:

circuitry adapted to transfer the data from the first bus to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

15. (Currently Amended) The bridge of claim 12, further comprising:
a third bus;
a fourth bus;
a third bus interface coupled to communicate with the third bus;
a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively pause the first buffer to store other data from the third and fourth bus interfaces.

16. (Currently Amended) The bridge of claim 12, wherein the heal bus interface further comprises:

a local bus controller adapted to use the first buffer to furnish signals to the local bus that indicate the data.

17. (Cancelled)

18. (Currently Amended) A method usable with a computer system that includes a local bus and a memory bus, the method comprising:

furnishing data to the memory bus in a memory read operation; ~~and~~

capturing the data directly from the memory bus in a first buffer that is located closer to the local bus than to the memory bus; and

furnishing other data to the memory bus from a second buffer that is located in a memory interface, the memory interface being located closer to the memory bus than to the local bus.

19. (Original) The method of claim 18, wherein the act of capturing comprises: latching the data from the memory bus in response to a data strobe signal of the memory bus.

20. (Currently Amended) The method of claim 18, further comprising:

using conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the first buffer to a second region located closer to the first buffer than to the memory bus, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

21. (Currently Amended) The method of claim 20, further comprising:

transferring the data from the first buffer to the local bus without introducing a second asynchronous propagation delay that 1s greater than the first asynchronous propagation delay.

22. (Currently Amended) A method usable with a computer system, comprising:

extending a memory bus into a bridge, the memory bus being adapted to indicate data in a memory read operation; ~~and~~

capturing the data directly from the extension of the memory bus into a first buffer of the bridge, the first buffer being located closer to a local bus than to the memory bus; and

furnishing other data to the memory bus from a second buffer located inside a memory interface, the memory interface being located closer to the memory bus than to the local bus.

23. (Original) The method of claim 22, wherein the act of capturing comprises: latching the data from the extension of the memory bus in response to a data strobe signal of the memory bus.

24.-25. (Cancelled)

26. (Currently Amended) The method of claim 22, wherein the act of extending comprises:

extending the memory bus into the bridge so that the extended end of the memory bus is closer to [[a]] the local bus than to the portion of the memory bus that is located outside of the bridge.

27, Currently Amended) The method of claim 18, further comprising: transferring the data from the first buffer to the local bus; and synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal,

28. (Currently Amended) The method of claim 22, further comprising: transferring the data from[[a]] the second buffer to[[a]] the local bus; and, ~~the buffer being located closer to the memory bus than to the local bus; and~~

synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

3. The following is an **examiner's statement of reasons for allowance**: the prior art of record does not teach or suggest a computer system arrangement in the context of the bridge as discloses in figures 6-7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xuong M. Chung-Trans whose telephone number is (703) 305-9772. The examiner can normally be reached on Monday-Friday from 9:30am to 1:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula Bradley, can be reached on (703) 308-2319. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

XM Chung-Trans

SUMATI LEFKOWITZ
PRIMARY EXAMINER